

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Previously presented): A method of fabricating an integrated circuit, comprising the following steps performed in order of:

- forming an interlevel dielectric layer over a semiconductor body;
- forming an intrametal dielectric layer over said interlevel dielectric layer;
- forming a hardmask over said intrametal dielectric layer;
- forming a via pattern over said hardmask;
- selectively etching a via through said hardmask;
- partially extending said via by selectively etching said intrametal dielectric layer;
- depositing a BARC layer over said hardmask and within said via, wherein said BARC layer is significantly thicker within said via than over said hardmask;
- forming a trench pattern over said BARC layer; and
- etching a trench in said intrametal dielectric layer, wherein said etching a trench step further removes at least a portion of said BARC layer within said via and removes a portion of said interlevel dielectric layer such that at the conclusion of said etching a trench step said via extends through said interlevel dielectric layer.

Claim 2 (Previously presented): The method of claim 1, further comprising the steps of forming a shelf layer between said interlevel dielectric layer and said intrametal dielectric layer; and extending said via by selectively etching through said shelf layer after said partially extending said via step.

Claims 3-5 (Canceled).

Claim 6 (Original): The method of claim 1, further comprising the step of filling said trench and via with copper.

Claim 7 (Original): The method of claim 1, wherein said intrametal dielectric layer comprises an organic polymer.

Claim 8 (Original): The method of claim 1, wherein said intrametal dielectric layer and said interlevel dielectric layer comprise SiLK™.

Claim 9 (Original): The method of claim 1, wherein said interlevel dielectric comprises an organic polymer.

Claim 10 (Previously presented): A method of fabricating an integrated circuit, comprising the following steps performed in order:

- forming an interlevel dielectric layer over a semiconductor body;
- forming a shelf layer over said interlevel dielectric layer;
- forming an intrametal dielectric layer over said shelf layer;
- forming a hardmask over said intrametal dielectric layer;
- forming a via pattern over said hardmask;
- selectively etching a via through said hardmask;
- partially extending said via by selectively etching said intrametal dielectric layer and said shelf layer, but not etching through said interlevel dielectric layer;
- depositing a BARC layer over said hardmask and within said via after said extending said via step;
- forming a trench pattern over said BARC layer; and
- etching a trench in said intrametal dielectric layer, wherein said etching a trench step further removes at least a portion of said BARC layer within said via and extends said via through said interlevel dielectric layer.

Claims 11-14 (Cancelled).

Claim 15 (New): A method of fabricating an integrated circuit, comprising the following steps performed in order of:

- forming an interlevel dielectric layer over a semiconductor body;
- forming an intrametal dielectric layer over said interlevel dielectric layer;
- forming a hardmask over said intrametal dielectric layer;
- forming a via pattern over said hardmask;
- selectively etching a via through said hardmask;
- forming a half via by extending said via through said intrametal dielectric layer using selective etching;
- depositing a BARC layer over said hardmask and within said via, wherein said BARC layer is significantly thicker within said via than over said hardmask;
- forming a trench pattern over said BARC layer; and
- etching a trench in said intrametal dielectric layer, wherein said etching a trench step further removes at least a portion of said BARC layer within said via and removes a portion of said interlevel dielectric layer such that at the conclusion of said etching a trench step said via extends through said interlevel dielectric layer.

Claim 16 (New): The method of claim 15, further comprising the steps of forming a shelf layer between said interlevel dielectric layer and said intrametal dielectric layer, wherein said step of forming a half via further extends said via through said shelf layer.